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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,058	12/16/2003	James W. Nicholes	1280-SC12980TC	5196
34814	7590	10/19/2005	EXAMINER	
TOLER & LARSON & ABEL, L.L.P. 5000 PLAZA ON THE LAKE SUITE 265 AUSTIN, TX 78746			NGUYEN, TAN	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary

Application No.

10/737,058

Applicant(s)

NICHOLAS, JAMES W.

Examiner

Tan T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-24 is/are allowed.
- 6) ☒ Claim(s) 1 and 6-12 is/are rejected.
- 7) ☒ Claim(s) 2-5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

1. The following action is in response to the amendment filed by Applicant on September 20, 2005.
2. The Information Disclosure Statement submitted by Applicant on July 25, 2005 has been received and fully considered. Reference "BD" to Hauser appears to be irrelevant to the present application.
3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohno (U.S. Patent No. 5,703,820).

Kohno disclosed in Figure 5 a memory device comprises a discharge circuit [9], which is composed of transistors [Q91-Q9n and Q9r], coupled to a plurality of digit lines [D1-Dn] and a reference digit line [DR], a timing signal [AT2] is supplied to the gates of all the transistors [Q91-Q9n and Q9r] (column 8, lines 62-67). Kohno disclosed in Figure 6 that when the timing signal [AT2] is set to the High level, the transistors [Q91-Q9n and Q9r] are set to be conductive state, as a result, charges of the digit lines [D1-Dn] and charge of the reference digit line [Dr] are all discharged to the ground potential level. At the same time, the logic gate [G61, G62] are inactivated, this time interval would be understood as the claimed inactive memory access period because the inactivation of these logic gates output a low level regardless of any input to the input terminals [S1] and [R1] (column 11, lines 19-29). Subsequently, when the timing signal

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[AT2] is set to the Low level, each transistor of the discharge circuit [9] is set to the non-conductive state, as a result, the discharge operation is not executed. Further, the logic gates [G61], [G62] of the sense amplifier [6] are activated, therefore the selected digit line and the reference digit line are charged (column 11, lines 35-41). The sense amplifier [6] compares and amplifies the information on the digit line [D1] with the information on the reference digit line [DR] and outputs the amplified result as a signal [SO] (column 10, lines 4-8).

- a. Regarding claims 6-7, Kohno disclosed in Figure 7 the reference digit line [Dr] is charge to the voltage of 1.5 volt, while the voltage of the selected digit line [D1] is equilibrated to the voltage V_{DOFF} of 1.55 V when the selected memory cell is an OFF bit, and to the voltage V_{DON} of 1.45 V when the selected memory cell is an ON bit (column 11, lines 50-55). Accordingly, the voltage difference is greater than 100millivolts or 150millivolts.

Regarding claim 8, Kohno disclosed the reference digit line [Dr] is charged as the timing signal [AT2] is set to low level (column 11, lines 39-40).

Regarding claim 9, Kohno disclosed the reference digit line [Dr] is discharged as the timing [AT2] is set to the High level, during which the logic gates [G61, G62] of the sense amplifier [6] are inactivated (column 11, lines 19-29).

Regarding claims 10-11, as shown in Figure 7, the selected digit line [D1] and the reference digit line [Dr] are charged from 0 V to about 1.45-1.50 V during the precharge period, which include the mid-point voltage level.

Regarding claim 12, Kohno disclosed the voltage of the selected digit line [D1] is equilibrated to the voltage V_{DOFF} of 1.55 V when the selected memory cell is an OFF bit, and to the voltage V_{DON} of 1.45 V when the selected memory cell is an ON bit (column 11, lines 50-55).

5. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Applicant's arguments with respect to claims 1-5, 8-9, 12 and 23 have been considered but are moot in view of the new ground(s) of rejection.

7. REMARKS

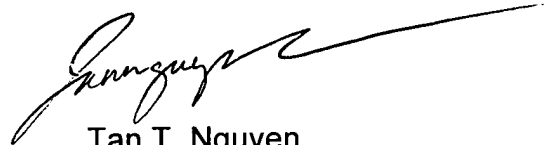
In view of Applicant's Remarks in the amendment, the 102 (b) Rejection under Hanriat et al. (U.S. Patent No. 6,282,114) to claims 1-5, 8-9 and 12 has been withdrawn. New reference to Kohno (U.S. Patent No. 5,703,820) has been found and applied to reject claims 1, 6-12 under 102 (b). Applicant is correct that the rejection to claim 23 was an error. In claim 1, Applicant claimed an "inactive memory access period" which would be understood as a memory access period during which the sense amplifier is not activated, accordingly, the Kohno reference meets this limitation.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
October 13, 2005